IN THE SPECIFICATION

Please amend paragraph 3 on page 6 as follows.

At this point, when the dynamic range of class tap is taken to be DR; the bit allocation is taken to be m, the [[data]] value of each class tap to be L; and the quantization code is taken to be Q, the ADRC circuit conducts the quantization by evenly dividing data between the maximum value MAX and the minimum value MIN into areas by the specified bit length, according to the following EQUATION (1).

Please amend Equation 4 on page 12 (paragraph 5) as follows.

~~$W[k+1] = 0.54 - 0.46*\cos(2\pi*k/N-1) \quad (k=0, \ldots, N-1)$ \quad (4)~~

$W[k]=0.54 - 0.46*\cos(2\pi*k/N) \quad (k=0,\ldots,N)$ \quad ... (4)